



STR17 - STM32L1

This course describe the STM32L1 architecture and practical examples

Objectives

- Understand Cortex-M3 core and STM32L1 SoC.
- Configure RCC (MSI/HSI/HSE/LSI/LSE) and PLL.
- Use GPIO/EXTI, timers, DMA, ADC, serial I/O.
- Apply ultra-low-power modes and measure impact.
- Manage Flash, true Data EEPROM, Option Bytes, watchdogs.
- (Variant) Bring up USB FS, LCD, TSC.

Course Environment

- Theoretical course
 - PDF course material (in English) supplemented by a printed version for face-to-face courses.
 - Online courses are dispensed using the Teams video-conferencing system.
 - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- Practical activities
 - Practical activities represent from 40% to 50% of course duration.
 - Code examples, exercises and solutions
 - For remote trainings:
 - ▶ One Online Linux PC per trainee for the practical activities.
 - ▶ The trainer has access to trainees' Online PCs for technical and pedagogical assistance.
 - ▶ QEMU Emulated board or physical board connected to the online PC (depending on the course).
 - ▶ Some Labs may be completed between sessions and are checked by the trainer on the next session.
 - For face-to-face trainings:
 - ▶ One PC (Linux ou Windows) for the practical activities with, if appropriate, a target board.
 - ▶ One PC for two trainees when there are more than 6 trainees.
 - For onsite trainings:
 - ▶ An installation and test manual is provided to allow preinstallation of the needed software.
 - ▶ The trainer come with target boards if needed during the practical activities (and bring them back at the end of the course).
- Downloadable preconfigured virtual machine for post-course practical activities
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

Day 1

Cortex-M3 overview (core)

- Core overview
- MSP/PSP stacks.
- Exceptions, NVIC priority.
- SysTick, SVC, PendSV.
- Faults: HardFault path.
- WFI/WFE basics.

Exercise: Exception Management

SoC & memory map

- Lines: L1x1/L1x2/L1x3.
- Flash/SRAM/PPB layout.
- Peripheral address map.
- UID and Flash size regs.
- Option Bytes snapshot.

Exercise: Map & IDs

RCC - reset & clocks

- MSI ranges/accuracy.
- HSI/HSE selection.
- PLL M/N/R (device).
- SYSCLK mux, AHB/APB.
- CCIPR kernel clocks.
- MCO output; CSS.

Exercise: Clock profiles

Power & voltage scaling

- Sleep/Low-power run.
- Low-power sleep/Stop.
- Standby + VBAT domain.
- Voltage scaling ranges.
- PVD/BOR.

Exercise: Mode sweep

GPIO / EXTI / SYSCFG

- PP/OD, pulls, speeds.
- AF mapping rules.
- EXTI lines, priorities.
- Debounce strategies.
- Safe I/O at reset.

Exercise: GPIO + EXTI

Timers (gen/basic) (LPTIM if present)

- PWM edge/center.

- Input capture.
- One-pulse mode.
- Encoder interface.
- Master/slave triggers.
- (Variant) LPTIM tickless.

Exercise: PWM + capture

Day 2

DMA

- Channels/requests map.
- Normal vs circular.
- HT/TC/TE flags.
- Throughput vs latency.

Exercise: UART RX ring (DMA)

ADC & analog

- 12-bit ADC basics.
- Sampling time, ranks.
- Timer-triggered ADC.
- DMA continuous/circular.
- Analog watchdog.
- Internal VREF/TEMP.

Exercise: ADC + DMA stream

RTC & tickless timing

- LSE vs LSI trade-offs.
- Calendar, alarm, wakeup.
- Backup registers.
- Tickless via RTC/LPTIM.
- Drift, calibration.

Exercise: Tickless blink

USART / LPUART

- USART Overview.
- Blocking/IRQ/DMA.
- Stop-mode wake (LPUART).
- Error recovery (ORE/FE).

Exercise: Robust UART

Exercise: LPUART wake from Stop

SPI

- CPOL/CPHA modes.
- Data sizes; NSS rules.
- Full-duplex DMA.
- Simplex options.
- Timing check (LA).

Exercise: SPI loopback DMA

I²C

- Sm/Fm/Fm+ speeds.

- 7/10-bit addressing.
- Analog/digital filters.
- Timeouts; bus-clear.
- Clock stretching.

Day 3

USB FS device (variant)

- VBUS sense options.
- EP/FIFO basics.
- CDC/DFU quick paths.
- Clocking constraints.
- Suspend/resume flow.

Exercise: CDC echo or DFU

LCD segment driver (variant)

- COM/SEG mapping.
- Bias/duty settings.
- Frame frequency.
- Contrast options.
- Simple icon drive.

Exercise: LCD icon demo

TSC capacitive touch (variant)

- Channel groups/IOs.
- Acquisition timing.
- Threshold tuning.
- Noise filtering.
- Key/slider basics.

Exercise: Touch key demo

Flash, Data EEPROM & OB

- Flash erase/program.
- True Data EEPROM use.
- Simple wear-leveling.
- OB: RDP/PCROP/BOR.
- Reset cause logging.

Exercise: EEPROM config

Boot, ROM & watchdogs

- ROM bootloader ports.
- DFU/UART/I²C options.
- Boot pins & OB links.
- IWDG vs WWDG basics.
- Reset causes record.

Exercise: IWDG + DFU try

Production checklist (wrap-up)

- Clocking proven (MCO).
- I/O safe at boot/sleep.
- Low-power numbers noted.

- Comms error policy set.
- UID/serial/CRC scheme.

Exercise: Self-audit