



## T1 - Tsi107 PCI bridge

*This course covers the Tsi107 PowerPC host bridge*

### Objectives

- The course details Tsi107 internal datapaths.
- The I2O synchronization mechanism is studied to clarify how multiple processors can synchronize to each other.
- SDRAM timing parameters initialization is described.
- The training explains how to use the DMA controller to transfer data from SDRAM to PCI space.
- This course has been delivered several times to companies developing defense equipments.

A more detailed course description is available on request at [training@ac6-training.com](mailto:training@ac6-training.com)

### Prerequisites & related courses

- Knowledge of PCI is recommended, see our course reference [IC1 - PCI 3.0](#) course
- ACSYS offers a large set of trainings on NXP and IBM Microelectronics PowerPC host CPUs.

### Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

### Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

## Course Outline

### OVERVIEW

- Clock generation, DLL benefits
- Memory mapping
- Explanation of the translation mechanism to access PCI MEM space
- Explanation of the translation mechanism used when PCI masters access the local SDRAM

### THE SDRAM CONTROLLER

- SDRAM basics
- Mode register initialization
- Command truth table
- Tsi107 memory controller introduction
- Address multiplexing
- The Flash EPROM controller
- X-port advantages and restrictions

## THE PCI INTERFACE

- Commands supported when the Tsi107 is PCI master
- Commands supported when the Tsi107 is PCI target
- Configuration space access through CONFIG\_ADDRESS and CONFIG\_DATA registers

## THE 60X INTERFACE

- 7XX or 74XX PowerPC connection
- 60X slave connection
- Error management

## THE INTERRUPT CONTROLLER

- EPIC operation modes
- Interrupt request time-multiplexing
- Interrupt nesting requirements
- Integrated timers
- Doorbell registers
- I2O specification basics, synchronization by messages

## THE DMA CONTROLLER

- Direct mode vs chained buffer mode
- Programming model
- Transfer descriptor initialization when the scatter / gather mode is selected

## THE I2C CONTROLLER

- I2C basics
- Interrupt driven communication sequence

## RESET

- Configuration pins sampling upon reset
- Initialization sequence