T2 - Tsi108 / Tsi109 PCI bridge

This course covers the Tsi108/109 PowerPC host bridge

Objectives

- The course describes the TSI108/109 internal data paths.
- The course explains how the host PowerPC and a CPU connected to PCI-X can synchronize to each other through the mailboxes.
- A long introduction to DDR2 SDRAM is done prior to describe the DDR SDRAM controller operation.
- The training explains how to implement chained DMA transfers.
- The course highlights the possible optimizations that can be implemented to boost the performance of the Ethernet controller.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites & related courses

- Knowledge of PCI / PCI-X is recommended, see our courses reference IC1 - PCI 3.0course and reference IC2 - Compact PCI course
- ACSYS offers a large set of trainings on NXP and IBM Microelectronics PowerPC host CPUs.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

OVERVIEW

- Switch fabric
- Parameterizing the crossbar
- Differences between TSI108 and TSI109

HARDWARE IMPLEMENTATION

- Power-up sequence
- Clock generator
- Programming the clock spread and modulation frequency

CPU INTERFACE

- Single (Tsi108) or dual (Tsi109) processor interface

- 60X and MPX bus modes
- Address remap
- Endian conversion
- Cache coherency
- Error logging

DDR2 INTERFACE

- Introduction to DDR SDRAM from Jedec specification
- Initialization sequence
- DDR2 SDRAM controller
- Page management
- Transaction ordering
- ECC and read-modify-write transactions
- DIMM support
- Low power modes

HOST LOCAL PORT INTERFACE

- Connection of 8-, 16- and 32-bit devices
- Timing parameters
- Burst transactions

PCI-X INTERFACE

- PCI or PCI-X selection option during reset
- Message Signaled Interrupts generation
- Compact PCI hot swap support
- Transaction ordering rules

GENERAL PURPOSE INPUT/ OUTPUT PINS

- Standard I/O port
- Event-latched input port

INTERRUPT CONTROLLERS AND TIMERS

- Priority levels
- Level / edge sensitivity selection
- Software based interrupt sources : doorbells, mailboxes and timers
- Delivery modes
- Nesting

I2C CONTROLLER

- I2C protocol basics
- Transmit sequence
- Receive sequence

DMA/XOR CONTROLLER

- Presentation of the 4 independent channels
- Direct mode operation
- Linked list mode operation
- XOR operations on multiple blocks of data
- Unaligned transfers

16550 COMPATIBLE UARTs

- Baud generation
- FIFO mode
- Transmit sequence
- Receive sequence

GIGABIT ETHERNET CONTROLLERS

- Interface to the PHY, GMII, MII or TBI mode
- Address filtering, utilization of hash tables
- Dedicated DMA, chained buffers
- Management interface, auto-negotiation
- VLAN packet filtering
- Priority tagging, virtual channels