



R2 - ARM11 implementation

This course covers ARM1136 and ARM1176 CPUs

Objectives

- This course is split into 3 important parts:
 - ARM11 architecture
 - ARM11 software implementation and debug
 - ARM11 hardware implementation.
- MMU operation under Linux is described.
- Interaction between level 1 caches, level 2 cache and main memory is studied through sequences.
- The exception mechanism is detailed, particularly the utilization of the VIC port.
- The course also details the hardware implementation and provides some guidelines to design a SoC based on ARM1136/76.
- An overview of the Coresight specification is provided prior to describing the debug related units.
- ACSYS has developed FFTs optimized for ARM11 coded in assembler language
 - performance for 1024 complex floating point single precision samples is 220_000 core clock cycles for VFP11 (ARM11)
 - performance for 1024 complex fixed point 16-bit samples is 206_000 core clock cycles (ARM SIMD V6 instructions)
 - for any information contact training@ac6-training.com

Labs are run under RVDS

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Knowledge of ARM7/9 or having attended the ARM fundamentals course.
- This course does not include chapters on low level programming.
 - ACSYS offers a large set of tutorials to become familiar with RVDS, assembly level programming, compiler hints and tips.
- More than 12 correct answers to ARM11 prerequisites questionnaire.

Environnement du cours

- Cours théorique
 - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
 - Cours dispensé via le système de visioconférence Teams (si à distance)
 - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Modalités d'évaluation

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.

- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés
- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.
 - En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

Plan

First day

ARM BASICS

- States and modes
- Exception mechanism
- Instruction sets
- Purpose of CP15

INTRODUCTION TO ARM1136JF-2 AND ARM1176JZF-S

- Block diagram
- Highlighting the instruction path and the data path
- Clarifying the usage of the 4 AHB / AXI ports
- Typical architecture of a SoC based on ARM1136/76

ARM11 CORE PIPELINE

- Pipeline stages
- Branch prediction
- Return stack
- Instruction memory barrier, use case

TRUSTZONE

- Objectives
- Clarifying the transitions between NS OS Secure Monitor Secure OS
- Consequences on caches and TLBs
- Secure boot, boot sequence
- Distinguishing the Secure vector table from the NS vector table
- Enabling / disabling invasive and non-invasive secure debug

V6 MMU

- Memory types
- Inner and outer cache attributes
- Data memory barrier, data synchronization barrier, use cases
- Objectives of the MMU
- Page descriptors
- Highlighting the new features of the V6 architecture regarding the MMU
- Locking entries in TLB
- Abort status, imprecise abort

Second day

LEVEL 1 CACHES

- Cache basics
- 4-way set associative caches, virtual indexing, page coloring
- Hit under miss capability
- Maintenance operations

TCM AND DMA CHANNELS

- TCM, address decoding
- DMA channels
- DMA state machine, interrupts
- DMA programming, using virtual addresses

AHB PROTOCOL (ARM1136 specific, on request)

- Centralized address decoding
- Address gating logic
- Arbitration, bus parking
- Address pipelining
- Retry response
- Split response

AXI PROTOCOL

- AMBA 3
- AXI protocol, the 5 communication channels
- Channel handshake mechanism
- Basic transactions, read burst, write burst
- Protection attributes
- Data buses, utilization of byte write strobes
- Unaligned transfers
- Response signalling, requirement of a default slave
- Atomic access, exclusive vs locked transfers
- ARMv6 load / store exclusive instructions
- Ordering model
- Slave parameters
- AXI interconnection architectures

HARDWARE IMPLEMENTATION

- Reset sequence, power on reset and warm reset timing diagrams
- Power management, run, standby and shutdown modes
- New dormant mode
- Interface to power manager

Third day

L220 / L210 CACHE

- Indicating the purpose of internal buffers
- Write allocate policies
- Write merging
- Event monitoring
- Cache maintenance operations
- Low power interface
- Register block

EXCEPTION MANAGEMENT

- The 3 interrupt controller models: simple controller, vectored controller and controller using the VIC port

- Benefit of the VIC port interface
- New feature regarding exceptions: low latency mode

ARM11 DEBUG

- Performance monitor
- Instruction breakpoints and data watchpoints
- Vector catch hardware
- Thread aware debug
- Halt mode vs monitor mode
- Debug communication channel

ARM11 REAL-TIME TRACE

- Coresight ETM11
- AMBA Trace Bus, trace port and Embedded Trace Buffer
- Instruction tracing
- Data tracing
- Programming ETM11CS

Renseignements pratiques

Renseignements : 3 jours