RI0 - AXI3 / AXI4 INTERCONNECT

This course covers the AXI bus protocol, described in ARM AMBA v3 and v4

Objectives

- This course details first the AXI3 protocol.
- New signals present in AXI4 are then described.
- The course explains the AXI4 stream protocol and indicates in which case this simplified protocol is suitable.
- AXI4-lite protocol is described.
- The NIC-301 interconnect IP is studied, clarifying synthesis options as well as software QOS parameterizing.
- AXI Coherency Extensions (ACE) new channels are explained through an overall introduction to snooping.
- The CCI-400 interconnect IP is described, highlighting the purpose of ACE-lite ports.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Knowledge of an interconnect, such as IBM CoreConnect or ARM AHB is recommended.

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Course Outline

FIRST DAY

AXI3 PROTOCOL

- ARM AMBA versions
- Basic read and write transactions, pipelining, data reordering
- Global signals, clocking, low power handshake interface
- Detailing address channel signals
- Detailing data channel signals
- Detailing response signals
- Ordering model
- Managing exclusive resources

AXI4 NEW SIGNALS

- QoS signalling, defining a per-transaction priority

- Multiple region signalling

AXI4 LITE

- Simpler control register-style interface
- Bursts of 1 data beat
- Conversion, protection and detection

AXI4 STREAM

- Objectives of this new protocol
- Byte stream example
- Merging and packing
- Downsizing / upsizing
- Packet transfer

NIC-301 AXI3 INTERCONNECT

- TrustZone support
- Programmable features, QoS
- Arbitration algorithms
- Programmer s model

SECOND DAY

INTRODUCTION TO CACHE AND TLB COHERENCY

- Cache organization
- Explaining the need for coherency
- Translation Lookaside Buffer
- Implementing an I/O MMU

AXI COHERENCY EXTENSION

- Signals added to the traditional 5 channels
- Explaining what is a shareability domain
- Using barriers, related ARM instructions
- The three additional channels
- ACE new transactions: explaining through sequences their utilization
- Distributed virtual memory
- ACE-lite subset

CCI-400 AXI4 ACE INTERCONNECT

- SoC architecture example
- Implementation in a Big/little system
- Performance monitoring unit
- TrustZone support
- QoS value arbitration and propagation
- Regulation of outstanding transactions
- QoS value based on latency measurement