STR3 - STR91X implementation

This course covers STR9 ARM-based MCU family

Objectives

- The course details the hardware implementation of the STR91x microcontrollers.
- The boot sequence and the clocking are explained.
- The course focuses on the low level programming of the ARM966 CPU.
- Practical labs on integrated peripherals are based on I/O functions provided by ST.

- Note that ACSYS does not sell emulation probes and IDEs. Consequently this course has not been designed to convince attendees to buy a particular IDE. The unique objective consists in providing sufficient knowledge to attendees so that they can successfully design a system based on STR9.

- This course has been delivered several times to companies developing embedded systems, such as industrial equipments.

A lot of programming examples have been developed by ACSYS to explain the boot sequence, the vector table and the operation of embedded peripherals.

- *They have been developed with 2 different IDEs : Keil and IAR.*
- *Consequently for on site course, it is up to the customer to select the IDE under which labs will be run.*

A more detailed course description is available on request at training@ac6-training.com

Prerequisites and related courses

- This course provides an overview of the ARM966 core. Our course reference cours R1 - ARM7/9 implementationdetails the operation of this core.
- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference cours IP2 - USB 2.0
  - Ethernet and switching, reference cours N1 - Ethernet and switching
  - CAN bus, reference cours IA1 - CAN bus

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Modalités d'évaluation

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.
- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés

- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.
  - En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

Plan

INTRODUCTION TO STR91XF

Overview

- ARM core based architecture
- Features of AHB and APB buses
- The main three blocks : platform, core and input / output peripherals

THE PROCESSOR CORE

THE ARM966E-S CPU

- Operating modes : user, system, super, IRQ, FIQ, undef and abort
- Pipeline, calculation of the CPI
- Branch cache
- Clarifying the data path
- Tightly Coupled Memories
- ARM vs Thumb instruction sets, interworking
- Stack management
- Benefits of condition set capability in ARM state
- C-to-Assembly interface
- Exception mechanism, handler table
- Debug facilities

PLATFORM

INFRASTRUCTURE

- AHB/APB Bridges, split transactions, error handling
- Internal 96 KB SRAM,
- Flash memory
- Program and erase sequences
- VIC Interrupt controller
- Wake-up / interrupt unit
- System timers : Real Time Clock, Watchdog timer

HARDWARE IMPLEMENTATION

- Low voltage detectors
- Clocking
- Reset causes
- Start-up sequence, fetch of the first instruction
- Low power modes
- External Memory Interface
- I/O Ports

INTEGRATED I/Os

NON COMMUNICATION ORIENTED INPUT / OUTPUT PERIPHERALS

- Timers
  - Output compare and input capture capabilities, force compare modes
  - One pulse mode
  - Output PWM mode, on-the-fly modification of the duty cycle
  - Input PWM mode, pulse measurement
- DMA controller
  - Request priority management between the 16 channels
  - Scatter / gather operation, transfer descriptor chaining
  - Error management
- Analog-to-Digital Converter
  - One-shot or continuous conversion
  - Analog watchdog with interrupt generation
- 3-phase induction motor controller
  - Tacho counter operating modes
  - Rotor speed measurement
  - Dead time generator

COMMUNICATION CONTROLLERS

- I2C interface
  - I2C protocol basics
  - Slave mode vs master mode
  - Support for DMA
- Synchronous Serial Peripheral [SSP]
  - SPI protocol basics
  - Queue mode operation
  - Transfer sequence
- UART
  - Queue operation mode
  - Hardware flow control
  - IrDA mode
  - Support for DMA
- CAN controller
  - CAN protocol basics
  - CAN controller organization
  - Message objects
  - Filtering of received messages
  - FIFO mode management
- USB slave interface
  - USB protocol basics
  - Buffer description block, buffer descriptor table
  - DMA controller used to move data between buffers and EndPoints
  - Endpoint initialization
- Fast Ethernet controller
  - 802.3 MAC basics
  - Connection to the PHY : MII bus
  - Management interface, auto-negotiation
  - DMA controller operation
  - Frame filtering
  - VLAN support
  - Error management

Renseignements pratiques

Renseignements : 4 jours