FC2 - MPC7400/10 implementation

This course covers NXP G4 Power CPUs

Objectives

- The course provides coding guidelines based on the knowledge of the instruction pipeline.
- Data flows between SDRAM, L1 caches and L2 cache are highlighted.
- Cache coherency protocol is introduced in increasing depth.
- Vector instructions and new C operators are viewed in detail.
- Data streams parameterizing is emphasized through an example.
- This course covers bus operation, either 60X or MPX mode.
- Through a FFT algorithm, the instructor shows how to vectorize processing and reduce execution time using data streaming.
- The internal performance monitor has been programmed so that different versions of the FFT algorithm implementation can be compared.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Plan du cours

MPC7400/10 PIPELINE

- Superscalar out-of-order execution
- Branch Target Instruction Cache
- Static vs dynamic branch prediction
- Coding guidelines

L1 AND L2 CACHES

- Cache basics
- PLRU L1 replacement algorithm, FIFO L2 replacement algorithm
- Hardware data cache flush
- Cache coherency based on snooping, the MEI, MESI and MERSI state machines

INTERNAL DATA FLOWS

- Data and instructions queuing mechanism to decouple bus operation and internal activity
- The Memory Sub System
- The load fold queue and the store miss merging

MPC7400/10 SPECIFIC UNITS

- Power management
- Performance monitor
- JTAG debugger
- Differences between 7400 and 7410

THE UISA LAYER

- User registers
- Branch instructions
- Integer instructions
- IEEE754 floating point standard
- Float instructions
- EABI introduction

THE VEA LAYER

- Cache related instructions
- Little-endian emulation
- PowerPC timers

ALTIVEC IMPLEMENTATION

- Altivec registers
- Vector load / store instructions
- Vector integer instructions
- Vector float instructions
- Vector permut instructions
- ANSI C extensions to support vectors
- Altivec implementation on 7400/10
- Data streams

THE OEA LAYER - MMU

- MMU goals
- Process protection
- Tablesearch, hash value
- MMU implementation in real-time sensitive applications

THE OEA LAYER EXCEPTION MECHANISM

- Supervisor registers
- Context saving through SRR0/SRR1 registers
- Handler table
- Exception nesting

MPC7400 HARDWARE IMPLEMENTATION

- Auto-check on power up
- Bus features : address pipelining, split transactions

- 60X bus cycles
- MPX data only transactions
- Synchronous SRAM technologies
- L2 bus interface