FF1 - MCF5x07 implementation

This course covers MCF5307 and MCF5407 ColdFire MCUs

Objectives

- The course describes the ColdFire assembly language and highlights differences from 68K instructions.
- An example of SDRAM controller initialization is provided.
- Interfacing with external devices is explained.
- The interrupt controller is viewed in detail.
- Interrupt driven DMA transfers are studied.
- A programming example has been developped for each internal peripheral (serial; I2C, timer).

- This course has been delivered several times to companies developing industrial and avionics systems.

A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of peripherals.
• They have been developed with Diab Data compiler and are executed under Lauterbach debugger.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Plan du cours

MCF5307 ARCHITECTURE

Overview

- Coldfire roadmap
- Differences between ColdFires and 68K processors
- 5307 block diagram
- Pinout
- Memory mapped I/O organization

V3 CORE

CORE ARCHITECTURE

- 5307 pipeline
- Programming model
- Addressing modes
- Instruction set
- Stack management, subroutine call and return
- C to assembly interface
- Exception management
- Internal SRAM
- 5307 cache operation

CORE DEBUG

- Intrusive vs non-intrusive debug
- BDM port
- Hardware breakpoints
- Trace port

PLATFORM

HARDWARE IMPLEMENTATION

- Dynamic bus sizing
- Address decoding
- Arbitration
- Burst cycles
- Bus error management

THE SIM MODULE

- The interrupt controller
- The software watchdog
- Reset, self-configuration
- Clock synthesis
- General Purpose I/O pins

THE MEMORY CONTROLLER AND THE DRAM/SDRAM CONTROLLER

- SRAM connection, chip-select programming
- DRAM / SDRAM basics
- The 5x07 (S)DRAM controller : address decoding, refresh rate definition, address multiplexing selection

INTEGRATED I/Os

THE SERIAL PORTS

- Asynchronous ports
- Transmit and receive sequences
- Synchronous port : I2C basics
- Transmit and receive sequences

THE DMA CONTROLLER

- Single address vs dual address transfers
- Hardware interface, hardware initiated transfers
- Programming model

THE TIMERS

- Capture mode
- Period selection
- Interrupt control

MCF5407 ENHANCEMENTS

MCF5407

- V4 core enhancements
- Instruction set additions
- Enhanced memories
- On-chip DMA and serial ports modifications