IC41 - IDT PES32NT24xG2 PCI e Gen 2 switch

This course explains the implementation of these PCIe gen2 switches

Objectives

- This course describes the hardware implementation of the switch.
- It explains the possible configuration of switch s port: transparent PCI-to-PCI bridge, Non Transparent endpoints and integrated DMA endpoints.
- Partitioning is clarified through use cases.
- Software configuration is detailed.
- Error management and switch event report is also studied.

- Note that AC6 has a long experience of teaching to companies developing avionics systems.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Knowledge of PCIe gen1 or gen2 is mandatory, see our related courses.

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Plan du cours

SWITCH ARCHITECTURE

- Stack, TLP routing, possible port splitting
- Switch core
- DMA modules

RESET AND INITIALIZATION

- Switch fundamental reset sequence
- Boot configuration vector
- SWMODE[3:0] configuration pins
- Enumeration software
- Runtime reconfiguration

LINK AND PHY OPERATION

- Lane reversal
- Link width negotiation in case of bad lanes
- Dynamic link width reconfiguration
- Link speed negotiation
- Link retraining
- Crosslink

HARDWARE IMPLEMENTATION

- Clocking, global reference clock and port reference clock
- Port global clocked mode, port local clocked mode
- Support of spread spectrum clocking

PARTITIONABLE PCI EXPRESS SWITCH

- Associating ports to form a completely independent PCIe switch
- Port configuration, transparent bridge, Non-Transparent (NT) bridge, DMA endpoint
- Multi-function ports
- Port operating mode change
- Highlighting ports supporting DMA function and port supporting NT function
- NT interconnect
- NT mapping table, address translation

DMA OPERATION

- DMA controller registers, remapping them in MEM space
- Descriptor format, list of descriptors
- Multicast support
- Halting or suspending a transfer

SWITCH CORE ARCHITECTURE

- Single VC
- Ingress buffers
- Egress buffers, head-of-line blocking
- Packet routing classes, inter- and intra-partition transfers
- Port arbitration
- Cut-through operation
- Request metering

SWITCH EVENTS

- Signaling an event occurred in one partition to the host processor of other partitions
- Internal error logic, emulating errors, integrated ECC protection
- Reporting errors using AER

MULTICAST

- PCIe multicast specification
- Address type header field
- Transparent multicasting, multicast BAR
- NT multicasting, address and requester ID overlay feature

CONFIGURATION SPACES

- Register organization, global address space
- Indirect access from any function configuration space
- Transparent PCI-to-PCI bridge proprietary registers
- NT endpoint registers
- Switch control and status registers