IC6 - HyperTransport 3.0

This course covers the HyperTransport 3.0 high-speed interconnect

Objectives

- Point-to-point interconnect benefits compared to shared busses are highlighted
- The hardware implementation is described
- The course focuses on the packet ordering rules
- The course describes the discovery sequence required to initialize the HyperTransport chain

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a high speed digital bus.

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Plan du cours

OVERVIEW

- Topology of a HyperTransport based board : cavern devices, tunnel devices and bridges
- Point-to-point interconnect approach
- Benefits of HyperTransport in comparison with PCI
- Key features of HyperTransport protocol

THE HARDWARE INTERFACE

- LVDS differential pairs
- Double Data Rate clocking
- Signal groups
- Impedance requirements
- Link transfer timing characteristics
- Detailed transfer timing budget
- FIFO sizing

LINK INITIALIZATION

- PWROK and RESET# shared signals
- IO chain initialization, finding the firmware ROM
- Scalable performance
- Determination of the link width
- Link frequency initialization

PACKET STRUCTURE

- Control packets : Request, Response and Information
- Objective of the Flush and Fence packets
- Data packets

TRANSFER PROTOCOL

- Objectives of ordering rules
- IO streams, host ordering requirements, downstream IO ordering
- Virtual channels

FLOW CONTROL MECHANISM

- Use of NOP packets
- Insertion of information packets within data packets
- Initialization and use of the counters

TRANSACTION EXAMPLES

- Routing packets
- Addressing, memory mapping
- Transfer of a Read Request packet and associated Read Response packet
- Transfer of a Posted Write packet
- Transfer of a broadcast packet
- Transfer of Flush and Fence packets
- Boolean semaphore management

CONFIGURATION ACCESSES

- Configuration type cycles, what is new compared to PCI
- The HyperTransport structure present in the capability list
- Use of these registers by the configuration software
- System management, command mapping, special cycles
- Interrupt management

DOUBLE-HOSTED CHAINS

- Sharing double-hosted chain vs Non-Sharing double-hosted chains
- Breaking the chain through software in the Non-sharing case

POWER MANAGEMENT

- Reporting power management events to the host bridge
- Signalling wakeup
- Determination of upstream and downstream directions

ERROR DETECTION AND HANDLING

- CRC calculated over 512 bit-times on link, CRC window
- Error conditions
- Error reporting

- Sync flooding

ISOCHRONOUS TRAFFIC

- Requirements for devices when they support isochronous packets
- Isochronous flow control

THE EIGHTH-GENERATION OPTERON PROCESSOR FROM AMD

- Integration of a DDR-SDRAM controller
- Building a SMP platform through HyperTransport links
- HyperTransport PCI-X tunnel
- HyperTransport IO hub cave

TEST OF A HYPERTRANSPORT PLATFORM

- Value provided by adding a connector into the design
- Check lists for electrical and protocol compliance
- PCB design considerations
- Benefits of analysis probe through the FuturePlus solution