II1 - DigRF and RFFE

This course covers DigRF and RFFE MIPI buses

Objectives

- The course starts with an overview of MIPI specification.
- Chapters are studied with a bottom-top approach, starting with M-PHY and ending with RFFE.
- DigRF protocol, particularly frame acknowledgment, is detailed.
- The course describes the DigRF startup sequence.
- Connection to the antenna via RFFE is explained, focusing on both physical layer and protocol.
- Test modes are also covered.
- Companies interested in attending this course must adhere to MIPI organization.
- This course has been designed for engineers in charge of SoC architecture, functional verification or silicon validation.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Basic knowledge on digital electronics.

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Plan du cours

INTRODUCTION TO MIPI SPECIFICATIONS

M-PHY

- Termination scheme
- Signaling schemes
- M-PHY type II modules
- Embedding clock into the bitstream, 8b10b coding
- DC-balancing, running disparity
- PHY state definition
- HS-MODE BURST Operation
- SYS-BURST operation
- Configuration attributes

- Test modes
- Electrical characteristics, eye-diagrams
- Jitter influence on LINE characterization
- Recommended test functionality

DIGRF INTERFACE

- Overview
- Physical layer based on M-PHY Type-II
- 8b/10b control character mapping
- Interface states
- Protocol
- Programming model

DEVICE DESCRIPTOR BLOCK (DDB)

- Services to transfer descriptor and configuration data between devices on a MIPI Interconnect
- Underlying interconnect requirements
- DDB-PDU format
- DDB protocol support for Level 1 and Level 2 services

RF FRONT-END CONTROL INTERFACE (RFFE)

- Two-wire, serial interface
- Point-to-multipoint connectivity
- Time-accurate triggering mechanisms
- MIMO configuration
- Operating states
- Physical layer
- Protocol layer
- Command sequences
- Broadcast messages
- Device enumeration, device identification