M7 - 440SPe implementation

This course covers AMCC 440SPe processor

Objectives

- The course explains how to design a 440SPe board, highlighting reset and clocking.
- The data flows between PCI-X, PCI Express and DDR SDRAM are described.
- The course explains how to configure the internal buses (PLB crossbar and PLB-to-OPB bridge).
- DDR SDRAM operation is described in order to understand both the electrical interface and the memory controller programming.
- Book E PowerPC architecture is studied, especially the MMU.
- The course provides examples of internal peripherals software drivers.
- Gigabit Ethernet controller is viewed in detail.

- A chapter on Linux porting can be appended on request.

Labs are compiled with Diab Data compiler and run under Lauterbach debugger.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.
- Knowledge of PCI-X bus is recommended, see our course reference cours IC3 - PCI-X 2.0.
- Knowledge of PCI Express bus is recommended, see our course reference cours IC4 - PCI Express 3.0.
- Knowledge of Gigabit Ethernet is recommended, see our course reference cours N1 - Ethernet and switching.

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Plan du cours

INTRODUCTION TO 440SPe

- Block diagram
- Internal bus organization : dual PLB, OPB, DCR
- Internal concurrent transfers examples
- Introduction to Integrated peripherals
- Hardware implementation
- 440SPe memory mapping
- Programming model

ON CHIP BUSES

- Introduction to CoreConnect
- 2-way PLB crossbar, programming
- Bus errors recovery from syndrome registers
- PLB performance monitor

440 CORE

- Pipeline
- Internal caches
- Speculative loads, storage ordering and synchronization : msync & mbar instructions
- MMU

BOOK E COMPLIANT CORE

- Programming model
- Branch instructions
- Addressing modes, load & store instructions
- Integer instructions
- 16-bit mac instructions to develop DSP algorithms
- Exception management
- Exception priorities
- Core timers
- PowerPC EABI
- JTAG debug
- Real time trace

CLOCKS, RESET AND POWER MANAGEMENT

- Clocks synthesizer
- PCI-X clocking
- PCI Express clocking
- Clock and power management
- Low power modes
- Reset signals
- Initialization software requirements
- IIC bootstrap controller : processor configuration through the IIC port
- PCI-X bootstrap configuration
- Peripheral software reset
- Booting from local ROM in Host bridge mode
- Booting from local ROM in Agent bridge mode
- Booting from PCI

L2 CACHE CONTROLLER & INTERNAL SRAM CONTROLLER

- L2 cache features
- Data movement between memory, L2 and L1 caches
- L2 cache programming
- SRAM controller

INTERRUPT CONTROLLER & GENERAL PURPOSE TIMERS

- Interrupt masking and acknowledgement sequences
- Critical interrupt handlers using vectorization
- Interrupts priority management
- General Purpose Timers

THE DDR-SDRAM CONTROLLER

- DDR-SDRAM operation
- Jedec specification basics
- Hardware interface, SSTL-2 termination logic
- Differences between DDR-I and DDR-II
- ECC error correction
- Introduction to the 440SPe DDR-SDRAM controller
- Page management unit
- Initialization sequence
- Hardware implementation

THE EXTERNAL BUS CONTROLLER

- External bus pinout, driver enables
- Dynamic bus sizing
- Timing parameters
- Device-paced transfers

THE PCI-X BUS CONTROLLER

- DDR PCI-X operation
- Host vs agent configuration
- Data flows : Read prefetch and write posting buffers
- Inbound transactions handling, Outbound transactions handling
- Error handling
- Arbitration algorithm
- Boot modes, initialization / Reset sequence
- Sleep mode entering
- PCI-Express to PCI-X bridging
- Message passing
- Interrupts and MSI

THE PCI EXPRESS INTERFACES

- 8-lane host interface
- 4-lane secondary interfaces
- Root complex vs EndPoint configuration
- PCI Express functional cores
- Hardware implementation
- Power management
- Error handling
- Messaging

THE FAST ETHERNET CONTROLLER

- 802.3 specification fundamentals : PHY and MAC layers
- 440SPE Ethernet controller organization
- PHY
- Flow control
- VLAN support
- Frame filtering
- Hash table usage in switch applications
- Memory Access Layer controller, buffer management
- Buffer descriptors initialization
- Errors management

THE XOR ACCELERATOR UNIT

- Parity generation and check functions
- Command block list
- DMA capability

THE I2O MESSAGE UNIT / DMA CONTROLLER

- Message vs doorbell
- Management of inbound messages
- Management of outbound messages
- DMA operation

STANDARD PERIPHERALS

- GPIO
  - GPIO interface signals
  - Pin configuration
- UART
  - FIFO mode
  - Flow control signals management
- IIC
  - IIC protocol fundamentals
  - Transmission and reception sequence
  - Serial boot ROM