



## NP2 - LPC17xx microcontroller implementation

*This course covers NXP Cortex-M3-based LPC17XX MCU family.*

### Objectives

- This course has 5 main objectives:
  - Describing the hardware implementation and highlighting the pitfalls
  - Describing the ARM Cortex-M3 core architecture
  - Becoming familiar with the IDE and low level programming
  - Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units
  - Describing independent I/O modules and their drivers.
- Note that this course has been designed from the architecture of the most complex LPC17XX device, the LPC1769.
- Consequently, a chapter has been designed by Acsys for each possible integrated IP.
  - According to the actual reference chosen by the customer, some chapters may be removed.
- Products and services offered by ACSYS:
  - ACSYS is able to assist the customer by providing consultancies. Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.
  - ACSYS has also an expertise in FreeRTOS porting and uIP /LWIP stack or Interniche stack integration.

This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

### Prerequisites and related courses

- This course provides an overview of the ARM Cortex-M3 core. Our course reference course [RM2 - Cortex-M3 implementation](#) details the operation of this core.
- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference course [IP2 - USB 2.0](#)
  - Ethernet and switching, reference course [N1 - Ethernet and switching](#)
  - CAN bus, reference course [IA1 - CAN bus](#)

### Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

### Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

# Plan du cours

## ARCHITECTURE OF LPC17XX MCUs

- ARM core based architecture
- Description of LPC17XX and LPC13XX SoC architecture
- Clarifying the internal data and instruction paths: AHB-lite interconnect, peripheral buses, AHB-to-APB bridges
- Integrated memories
- SoC mapping

## THE ARM CORTEX-M3 CORE

- V7-M core family
- Core architecture
- Programming
- Exception behavior, exception return
- Basic interrupt operation, micro-coded interrupt mechanism
- Wakeup Interrupt Controller
- Memory Protection Unit

## BECOMING FAMILIAR WITH THE IDE

- Acsys covers 3 IDEs: Keil, IAR and GCC / Lauterbach.
- Thus the customer has just to indicate which one he has chosen
- Getting started with the IDE
- Creating a project from scratch
- C start program

## PROGRAMMING AND DEBUGGING

- Debug interface
- Programming

## RESET, POWER AND CLOCKING

- Power control
- Reset
- Clocking
- Low power modes

## INTERNAL INTERCONNECT

- AHB multi-layer matrix
- DMA

## HARDWARE IMPLEMENTATION

- Power pins
- Pinout
- GPIO module
- External Interrupts

## INTEGRATED MEMORIES

- Embedded flash memory

- On-chip static SRAM

## **TIMERS**

- Timers 0, 1, 2 and 3
- PWM
- Motor Control PWM
- Quadrature Encoder Interface
- Real Time Clock and backup registers
- Watchdog timer

## **ANALOG MODULES**

- 12-bit Analog-to-Digital Converter
- 10-bit Digital-to-Analog Converter

## **CONNECTIVITY AND COMMUNICATION**

- SPI
- SSP interfaces
- I2S interface
- UART
- I2C
- CAN controllers
- USB FS
- Fast ethernet