P3 - PPC464 core implementation

This course covers the IBM Power 464 core

Objectives

- A boot firmware that initializes the MMU has been developped to explain the boot sequence.
- Internal debug facilities are described.
- The course focuses on PPC464 low level programming, especially the PowerPC EABI.
- Examples of exception handlers are provided.
- A DFT has been developed to explain how to use MAC instructions.
- The Floating Point Unit operation is described.
- The PLB ports as well as debug related signals are described to facilitate the hardware implementation.

- This course has been delivered several times to engineers developing ASICs based on PPC464.

Labs are compiled with GNU compiler and run under Lauterbach Trace32 debugger.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Plan du cours

INTRODUCTION TO PPC464FP-H90

- Internal architecture overview
- Highlighting instruction and data paths
- Clocking
- Programming model, the 4 register groups GPRs, SPRs, DCRs and memory mapped
- CoreConnect-based SOCs

THE CORE ARCHITECTURE

- Pipeline basics
- 7-stage pipeline operation
- Speculative execution, guarded memory

- Serialization
- Cache basics
- Cache programming interface
- Process vs thread
- Memory Management Unit
- 36-bit real address space
- Translation Lookaside Buffer initialisation
- Cache control and debugging features
- Load / store buffer, speculative loads, msync and mbar instructions

BOOK E COMPLIANT CORE

- Booke E objectives
- Branch instructions
- Addressing modes
- Load / store instructions
- Semaphore management with lwarx / stwcx. Instructions
- Arithmetical and logical instructions, shift and rotate instructions
- Floating point unit, compliancy with IEEE754
- Processing denormalized FP numbers
- Floating point arithmetic instructions
- FP-to-integer and integer-to-FP casting
- The PowerPC EABI
- Cache related instructions
- 16-bit mac instructions to develop fixed point DSP algorithms
- 2-cycle multiply option
- Exception processing
- Critical versus non critical interrupts
- Syndrome registers updating when an exception is taken
- Core timers : PIT, FIT and WDT

INTEGRATED DEBUG FACILITIES

- JTAG emulator use
- The 464 instruction trace port
- Real time trace when the PowerPC core executes cached instructions
- Hardware vs software breakpoints

HARDWARE IMPLEMENTATION OF THE PPC464 CORE

- Signal naming convention
- External connections
- Clock and power management interface
- CPU control interface
- Reset interface
- External interrupt controller interface
- Instruction-side PLB interface
- Data-side PLB interface
- DCR interface